

# High Efficiency Light-Emitting Transistor with Vertical Metal–Oxide Heterostructure

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The monolithic integration of light-emission with a standard logic transistor is a much-desired multifunctionality. Here, a high-efficiency light-emitting transistor (LET) employing an inorganic quantum dots (QDs) emitter and a laser-annealed vertical metal–oxide heterostructure is reported. The experimental results show that the peak efficiency and luminance of this QDs LET (QLET) are 11% and 8000  $\text{cdm}^{-2}$ , respectively at a monochromatic emitting light wavelength of 585 nm. As far as it is known, these are among the highest values ever achieved for LETs. More importantly, the QLET exhibits an ultrahigh electron mobility of up to  $25 \text{ cm}^2 \text{ V}^{-1} \text{ S}^{-1}$ , a lower efficiency roll-off (7% at high  $3000 \text{ cdm}^{-2}$ ), and excellent stability with long-duration gate stress switching cycles. Additionally, this approach is compatible with those used in conventional large-area silicon electronic manufacturing and can enable a scalable and cost-effective procedure for future integrated versatile displays and lighting applications.

semiconductor channel shows unique light-emitting properties such as relatively high external quantum efficiency (EQE), perfect recombination ratios without light absorption by the metal electrodes.<sup>[5,6]</sup> In these devices, the trade-off between high EQE and high luminance with high device mobility or current density is often regarded as an obstacle which prevents organic light emitting transistors (OLETs) from extensive application. Consequently, OLETs usually experience a quick and drastic roll-off of efficiency at required high light-emitting luminance and excellent electrical performance.

Techniques involving quantum dots (QDs) and light-emitting diodes have been proven to be beneficial to powerful visualization and lighting methods.<sup>[7–11]</sup>

Light-emitting devices using high pho-

toluminescence quantum yield (PLQY) QDs as inorganic crystalline emission sources has many inherent advantages, such as size-tunable emission wavelengths, narrow emission line-widths (<60 nm), high quantum efficiency (5–20%) even at ultrahigh luminance ( $50\,000 \text{ cdm}^{-2}$ ).<sup>[12–15]</sup> Unfortunately, demand for high device mobility or current density (usually ten times more than that of OLED) is the only crucial difficult for QDs LET (QLET) fabrication. It is suspected that organic semiconductor cannot provide such high motility. Therefore, few reports about integrated QLET have revealed how to increase device's efficiency roll-off point. Several inorganic materials, such as ZnO and  $\text{TiO}_2$  nanoparticles (NPs), have been utilized as QLED's electron-transport layers (ETLs) and hole blocking layers, even though these discrete and non-uniform NPs' layers are not appropriate candidates for high device mobility transistor.<sup>[16]</sup> This difficulty results from the low mobility of the NPs layer and high leakage current from solution processing as well as a low electron tunneling efficiency.<sup>[17]</sup>

Recently, other nonplanar transistors in reported letters based on inorganic heterostructure (such as  $\text{CdS}$ <sup>[18]</sup> and metal–oxide (indium zinc oxide (IZO),<sup>[4]</sup> zinc tin oxide (ZTO)<sup>[5]</sup>) shows very high mobility ( $13\text{--}20 \text{ cm}^2 \text{ V}^{-1} \text{ S}^{-1}$ ) and luminance intensity ( $500 \text{ cdm}^{-2}$ ) at relatively high EQE ( $10^{-5}\text{--}10^{-2}\%$ ) with excellent gate's modulation capability, and it is possible to develop QLET with these semiconductor components. Moreover, emitting light can only escape at the edge of these devices' channel ( $\approx 30 \mu\text{m}$  lighting zone), the performance of which can be improved by using vertical metal–oxide heterostructure with deposited

## 1. Introduction

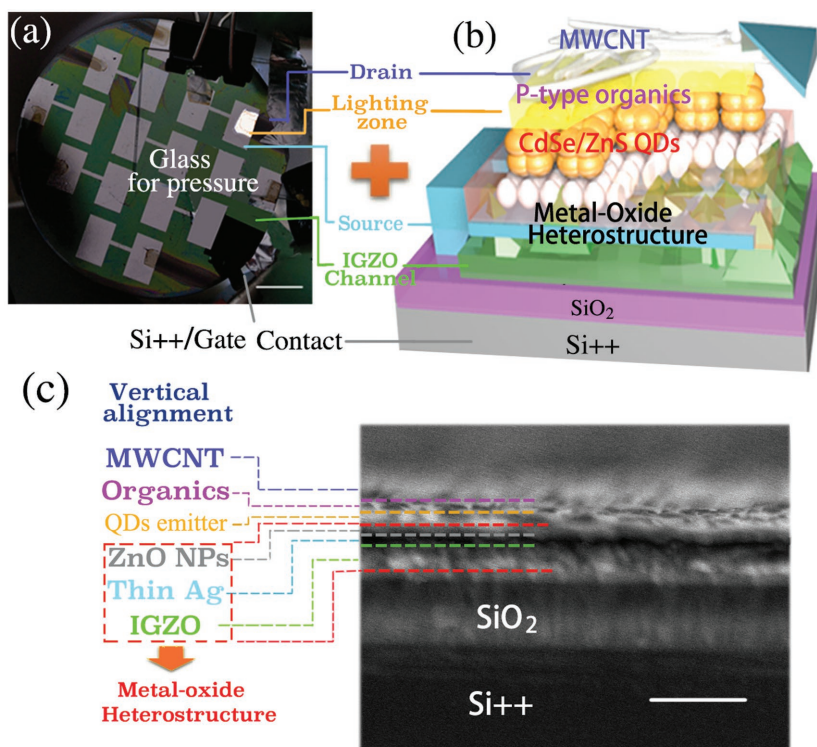
Light-emitting transistors (LETs) integrated with transistor and display pixels (especially for organic light-emitting display (OLED)) has emerged during the past few years due to their light-emitting/display properties and standard logic multifunctionality.<sup>[1–4]</sup> In contrast to a conventional planar transistor, light emitting transistors have been demonstrated with a combination of N-type and P-type transport semiconductor components, especially that made of organic materials.<sup>[3,4]</sup> So far, the vast majority of OLET devices with organic

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**Figure 1.** Schematic diagrams of device structure. a) Top-view image of the QLET device emitting high luminance light. b) Schematic diagram of this LETs with vertical alignment. c) Cross-sectional SEM image of QLET's lighting cell, scale bar = 0.2  $\mu\text{m}$ .

interlayer in the channel.<sup>[19]</sup> In vertical QLET device, the gate terminal can also modulate the carriers' injection efficiency to light emitting center, regulate the drain-source current and filter some noise dark current from source electrode through this intrinsic vertical heterojunction. Meanwhile, as a popular ETL in QLED stack, ZnO NPs can guarantee efficient electrons' injection and hole' blocking capabilities, which also have an excellent lattice matching and less trap states contacted with similar zinc-related material (indium gallium zinc oxide, IGZO). Additionally, EQE can also be increased by introducing light emitter made of high-efficiency inorganic QDs associated with this metal-oxide heterostructure.

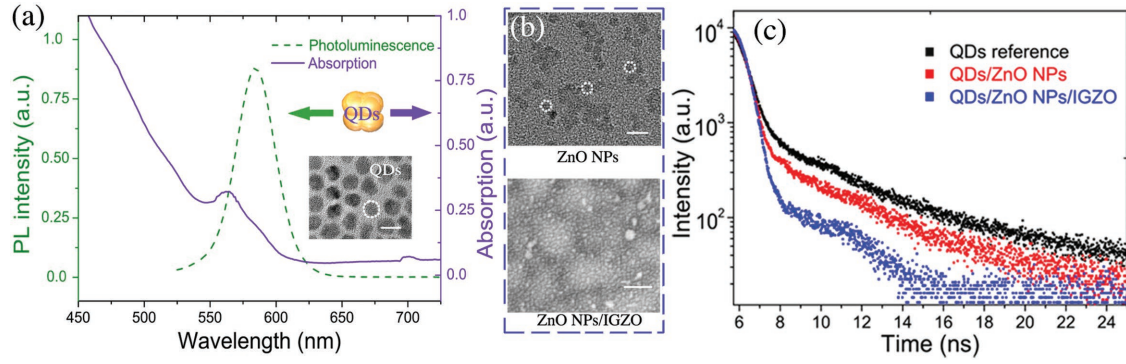
To accommodate this key feature of QLET, the most popular high mobility oxide semiconductor IGZO and vertical heterostructure architecture<sup>[20–24]</sup> are employed in this manuscript, which can provide a high current density and makes the fabrication of a QLET device possible due to its extraordinary electrical performance, such as high mobility ( $17\text{--}45\text{ m}^2\text{ V}^{-1}\text{ S}^{-1}$ ), low off current, low threshold voltage, high subthreshold slope (SS), and high on/off ratio.<sup>[24–26]</sup> As reported in previous research on OLET devices, sputtered thin metal layer,<sup>[27]</sup> evaporated and etched periodic metal<sup>[28,29]</sup> or certain spin-coated nanoelectrodes (such as indium tin oxide (ITO) or graphene)<sup>[20]</sup> at the channel area are applied in some vertical LETs to increase lighting area. Therefore, in this vertical transistor,  $\approx 30\text{ nm}$  Ag was sputtered within laser annealed IGZO clusters channel to increase lighting area in one hand and guarantee sufficient contact between active layer (IGZO) and ETL (ZnO NPs). The top-view and cross-sectional scheme of this nonplanar QLET

are illustrated in **Figure 1a–c** demonstrate: poly-silicon gate/ $\text{SiO}_2$  dielectric/IGZO channel layer/thin porous Ag contact/QLED stack/carbon nanotube (CNT) drain transparent contact. This metal-oxide heterostructure and charge transfer within interface are developed and studied by using metal-oxide-semiconductor (MOS) structure. Thanks to the bandgap extension of ZnO NPs and the charge transfer heterojunction between IGZO and ZnO NPs, the QLET possesses an excellent gate modulation capability with high mobility and stability. Additionally, high-efficiency inorganic QDs emitter also benefits from this and achieves good luminance, high EQE, and low efficiency roll-off.

## 2. Results and Discussion

In vertical transistor, the macroscopic device-mobility, threshold voltage, and other electrical performances are dominated by the charges' transport within the vertical heterostructure; that is, heterostructure can scatter carriers being transferred between drain/source electrodes, surface defects can lead to extra trap states, and heterojunction will act as carriers' transport barrier. **Figure 2a** shows optical photoluminescence and absorption spectra of CdSe/ZnS QDs which illustrates a discerning feature with a narrow emitting peak at 585 nm. It also indicates that QDs can be an excellent light emitting center with high PLQY ( $>80\%$  for our QDs) and pure monochromatic light. Furthermore, with illuminated at ultraviolet-to-green wavelengths light, QDs can absorb photons and generate electron-holes' carriers. To provide a preliminary investigation with charges' transport through quenching of light emission, time-dependent photoluminescence (PL) excited at 400 nm UV lamp was investigated to show the radiative lifetime of pristine QDs reference and its composites (QDs/ZnO NPs and QDs/ZnO/IGZO, can be seen in scanning electron microscope (SEM) image of **Figure 2b**). In the present investigation, the light emission decay kinetics of these nanocomposites on Si/ $\text{SiO}_2$  substrates are shown in **Figure 2c** and can be fitted first-order exponentially under room temperature. The time constants of  $\tau$  are at 5, 4.1, and 2 ns respectively for QDs reference, QDs on ZnO NPs layer, and QDs on ZnO NPs/IGZO hybrid layer. It is clearly seen from **Figure 2c** that light emission of QDs on ZnO NPs/IGZO surface decays much faster, which leads to a clear indication of charges' transport from excited QDs. Moreover, the faster free photocarrier's lifetime of QDs/ZnO NPs/IGZO composite appears due to this facilitating carrier's quenching at interface, because IGZO has much higher mobility than ZnO NPs. These are preliminary findings for charge's transport between the semiconductor components of this device. And more researches for the heterojunction and their impact on device performance will be specialized and exploited later.

The morphologies and structural properties of IGZO films were further observed and characterized by SEM and atomic force

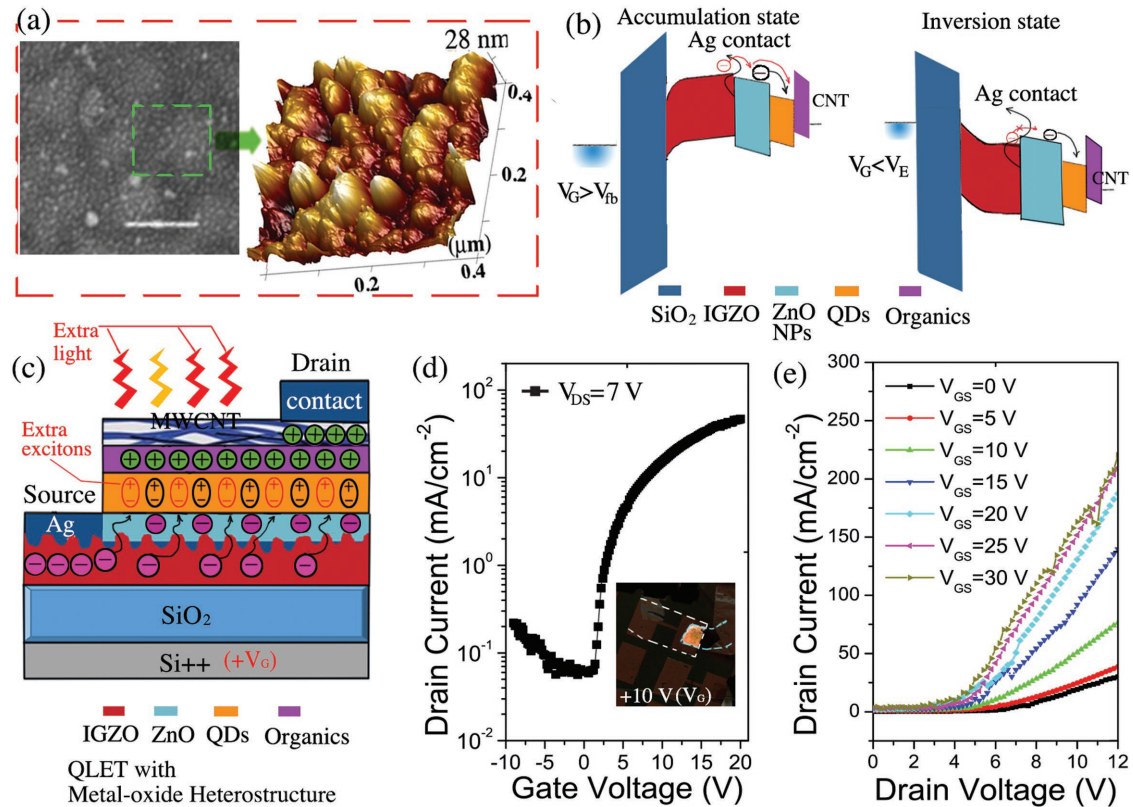


**Figure 2.** Characterization of semiconductor components in device. a) Absorption and PL spectrum for the CdSe/ZnS QDs emitter. b) TEM image of the ZnO NPs (scale bar: 5 nm) and ZnO NPs/IGZO hybrids (scale bar: 500 nm), CdSe/ZnS QDs and ZnO NPs (scale bar: 5 nm). c) Time-resolved PL spectrum for QDs reference layer, QDs/ZnO NPs, and QDs/ZnO NPs/IGZO hybrid after exciting at 400 nm.

microscope (AFM), as shown in **Figure 3a**. Many grains or clusters (height is around 30 nm as shown in AFM image of Figure 3a) remarkably emerged due to sintering process by lasers' annealing. It indicates that crystallized phase of as-deposited amorphous IGZO film was changed through this annealing process,<sup>[30,31]</sup> which can also be demonstrated by X-ray diffraction patterns in Figure S2 (Supporting Information) to reveal IGZO film's crystallization by the intensity peaks. With increasing of annealing laser's luminous energy, appear of typical sharp diffraction peaks implies crystallization of IGZO especially at laser's  $350 \text{ mJ cm}^{-2}$  high energy density. A conformal sputtering process was carried out to

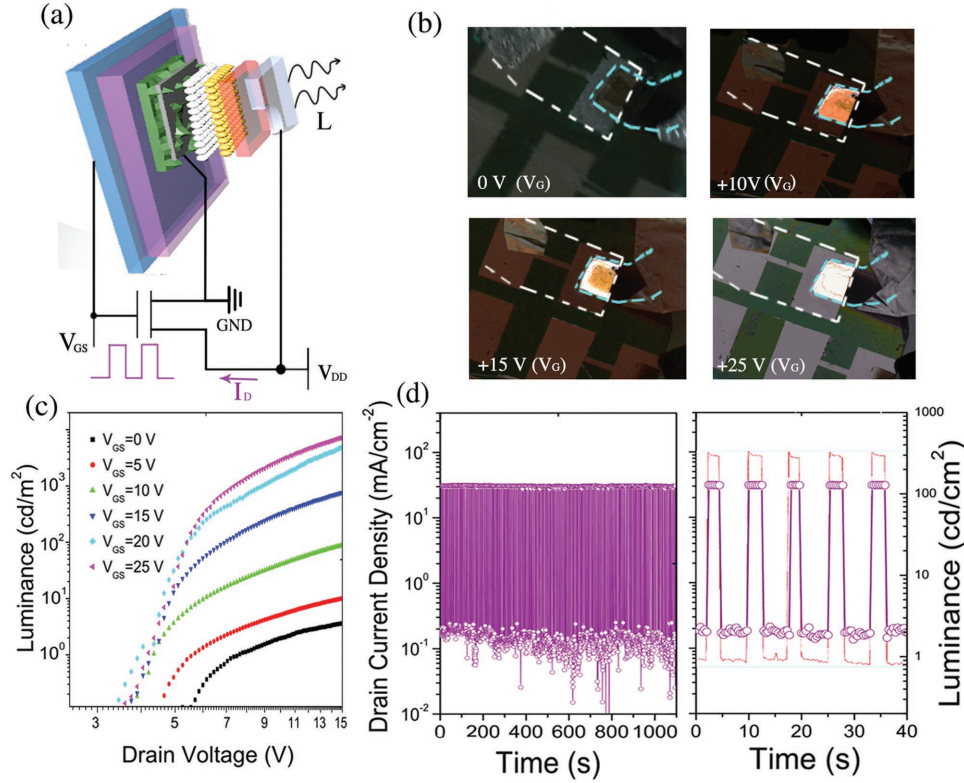
deposit thin Ag electrode and form a porous source electrode (can be seen in SEM image of Figure S4b in the Supporting Information). This source terminal can drive electrons toward QDs emitter along nanocluster (according to device architecture and carriers' flow in Figure 3c). Due to the principle of charge conservation, top-assigned multi-wall carbon nanotube (MWCNT) can also provide same amount of holes and cause electron-hole recombination in QDs emitter to generate extra light as shown in Figure 3c.

As witnessed in Figure 3d,e, the QLET's transfer and output characteristics are measured and plotted, where this device's mobility can be calculated by following expression:



**Figure 3.** Characterization and investigation of QLET device. a) SEM image of IGZO ( $350 \text{ mJ cm}^{-2}$ ) and AFM image to reveal the height information (inset). b,c) Schematic diagrams of bandgap alignment, transistor's vertical architecture, and carriers' flow. d) Transfer characteristics of QLET under  $V_{DS} = 7 \text{ V}$  and device lighting image by  $V_{GS}$ . e) Output characteristics of QLET under different gate voltage.





**Figure 4.** Electrical and Optical characterization of the QLET. a) Schematic diagram of the QLET and the peripheral circuits to measure the device. b) Photographs are the QLET pixel at different gate voltages and the same drain voltage (7 V). c) Relationship between the drain voltage and luminance ( $\text{cd/m}^2$ ). d) Current density of the vertical LET as a function of long-duration gate stress's switching cycles and response of optical luminance following with gate.

$$\mu = \frac{L}{W} \frac{1}{C_i V_{SD}} \frac{\partial I_D}{\partial V_G}. L \text{ and } W \text{ are the sizes of the channel, } V_{SD} \text{ is}$$

set up as 7 V, and  $C_i$  is the geometry capacitance of the gate insulator. The partial differential of drain current  $I_D$  with gate voltage  $V_G$  can be calculated by the transfer  $IV$  characteristics. As can be seen in Figure S4a in the Supporting Information, depositing 30 nm thick Ag can combine the best of transistor to attain excellent electrical performances such as device electron mobility ( $25 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ), SS ( $1.8 \text{ V Dec}^{-1}$ ), threshold voltage (5 V), and on/off ratio ( $\approx 10^3$ ). As shown in the comparable transfer curve of the QLET (Figure S4c, Supporting Information),  $V_{DS}$  has an enormous impact on the performance of the QLET (low on/off ratio and high SS). More specifically, with a high  $V_{DS}$ , the modulation phenomenon of the gate terminal is not obvious, as a high  $V_{DS}$  usually causes a high off current while the device reaches saturation.

Simultaneously,  $V_{DS}$  is held from 0 to 12 V with sweeping gate voltage between 0 and 30 V, as witnessed in output characteristics of Figure 3e. The distinct cut-off and linear regimes can be observed in this gate range. But obviously, this LET cannot reach saturation regime because the limit of current in QDs emitter layer. Figure 3b schematically explains the current modulation mechanism of the vertical QLET from the heterojunction's bandgap alignment of this vertical transistor. When a negative bias is applied (especially lower than equilibrium voltage,  $V_G < V_E$ ), this field effect transistor can work at inversion state, more minority holes can gather at

IGZO semiconductor. The bend of bandgap can decrease conduction band ( $E_C$ ) of IGZO and increase the electron's transport barrier height. When a positive gate bias (especially higher than flat band voltage,  $V_{GS} > V_{fb}$ ), this transistor works at accumulation state, more electrons can be induced and accumulated in IGZO semiconductor. It is evident from the increase of  $E_C$  (IGZO), and decrease of barrier height to benefit electrons' injection.

The photographs of the illuminating QLET illustrate that the brightness of QLET can increase with gradually applying higher gate voltage as shown in Figure 4b. Note that a large lighting area ( $4 \text{ mm}^2$ ) can be achieved using this vertical transistor structure. This value is much higher than the usual lighting area of reported OLET listed in Table 1. Furthermore, the measured luminance curve versus  $V_{DS}$  is plotted under different gate voltages in Figure 4c. In addition, by dividing by the luminance of the QLET under a small gate voltage, a large luminance on/off ratio ( $\approx 10^4$ ) can be realized. More importantly, applied by high gate voltage and drain voltage, the maximum luminance of this QLET is at  $8000 \text{ cd/m}^2$ , which is the highest among that of reported OLET, as shown in Table 1.

Figure 4d shows the drain current density of QLET during on/off gate's modulation (on: 15 V, off: 0 V) with continuous long gate bias time ( $>1000 \text{ s}$ ). The stability of IGZO helps to output robust drain current signal and keeps no noticeable change after long duration under on-state gate bias. The correlating luminance response to this 15 V on/off gate's modulation

**Table 1.** Summary of the electrical and optical properties of LETs.

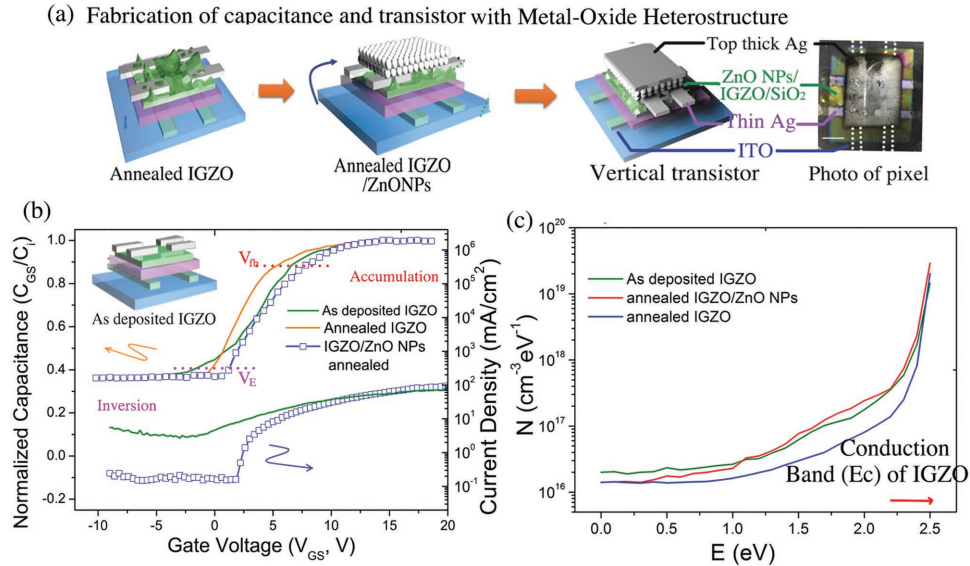
	Mobility [ $\text{cm}^2 \text{V}^{-1} \text{S}^{-1}$ ]	$V_{\text{th}}$	Luminance [ $\text{cdm}^{-2}$ ]	EQE [peak]	Lighting zone	FWHM [nm]	Ref.
This QLET	25	5 V	8000	11%	4 $\text{mm}^2$	60	
High-k OLET	0.42	-11 V	300	3%	$\approx 50 \mu\text{m}^2$	>200	[3]
PBTTT QLET	0.0252	-60 V	740	0.3%	$\approx 500 \mu\text{m}^2$	90	[33]
CdS OLET	19.5	15	419	$10^{-5}\%$	$\approx 35 \mu\text{m}^2$	300	[18]
IZO OLET	13	17	n/a	$10^{-6}\%$	$\approx 40 \mu\text{m}^2$	400	[4]
ZTO OLET	12.5	20	329	$10^{-3}\%$	$\approx 25 \mu\text{m}^2$	250	[5]
IGZO OLET	4.2	8 V	$\approx 2000$	0.5%	$\approx 0.1 \text{mm}^2$	120	[32]
ZnO/porous Si Naowire OLET	n/a	8 V	n/a	n/a	<625 $\mu\text{m}^2$	150	[23]

(response time < 10 ms) is also examined in Figure 4d, which shows an excellent optical following property with proportional to electrical gate signal. It attaches great significance to future high frequency and resolution display application. The last but not the least, attributed to the gate compensate effect, on-state drain current can be regulated with better stability than that of off-state drain current (without gate bias) in a long period. It is difficult to guarantee that all the pixel has the same turn-on voltage with large-area solution-processes, and which can cause nonuniformity of lighting or display. Therefore, except for driving functionality, at some large-scale display applications with mentioned solution-process, the vertical QLET structure can be applied to compensate lighting cells' current. It can make sure that all the pixels can emit light and be of similar luminance.

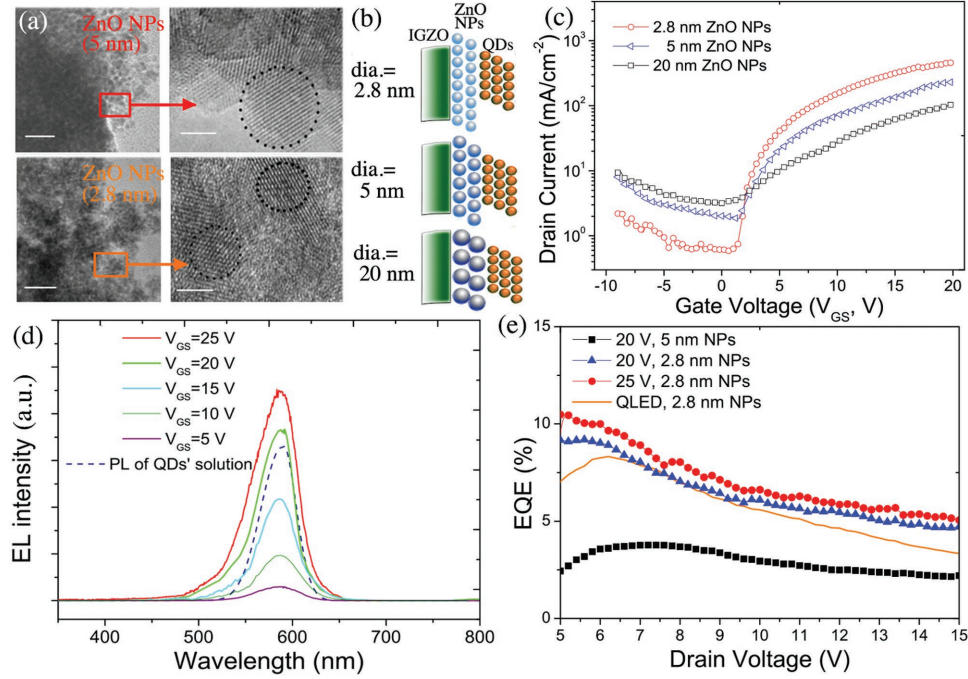
To fully analyze the operating mechanism of QLET and this metal-oxide heterostructure, the same plasma enhanced chemical vapor deposition (PECVD) and radio-frequency (RF) sputtering methods are utilized to deposit  $\text{SiO}_2$  and IGZO over the patterned ITO glass substrate as shown in Figure 5a and Figure S2a (Supporting Information). It can selectively rule

out the influence of heavy doped P-type silicon substrate and research C-V characteristics of MOS part in this device. Usually for other reported LETs, researchers directly introduce one insulator, which plays an important role in gate modulation. Strictly speaking, the gate modulation structures of those reported vertical LETs<sup>[20,25,29]</sup> are more accurately called as metal-insulator-metal (MIM) structure. On the contrary, the IGZO interlayer in our work helps to construct a MOS structure, which is measured and compared with an MIM structure counterpart as shown in Figure 5c and Figure S4 in the Supporting Information. The C-V curves of MOS capacitors can be used to resolve the corresponding kink transfer current behavior of vertical transistor as illustrated in Figure 5c. A positive flat-band voltage ( $V_{\text{fb}}$ ) is induced by the work function difference between ITO and N-type IGZO. And a small normalized inversion capacitance is brought about by the minority holes which are too slow to accumulate at  $\text{SiO}_2/\text{IGZO}$  interface with responding to such quick 1 MHz gate modulation in time.

Interestingly, compared with annealed IGZO sample, a negative shift of  $V_{\text{fb}}$  and a positive shift of  $V_{\text{E}}$  (voltage at equilibrium state, green curve in Figure 5b) can be observed in as-deposited



**Figure 5.** a) Fabrication and photograph of IGZO/ZnO NPs MOS capacitor and vertical transistor, scale bar: 100  $\mu\text{m}$ . b) C-V characteristics of MIS capacitor at high  $f = 1$  MHz and transfer  $I/V$  curves of vertical transistors with different IGZO layers. c) Trap densities of MOS capacitor's trap states versus surface energy potential, with different structures extracted from C-V curves.



**Figure 6.** a) TEM (scale bar: 20 nm) and HRTEM images of ZnO NPs with 5 nm diameter, scale bar: 2 nm; TEM (scale bar: 20 nm) and HRTEM images of ZnO NPs with 2.8 nm diameters, scale bar: 2 nm. b) Corresponding band structure of ZnO NPs to show the band gap extension with decrease of NPs' size. c) Transfer characteristics of QLET with different sizes of ZnO NPs. d) Electroluminescence spectra of QLET with 2.8 nm ZnO NPs in metal-oxide heterostructure and comparable PL of QDs. e) EQE Comparison of the as-fabricated QLET (with  $V_{GS} = 20$  V and different size of ZnO NPs) and conventional QLED pixels (inset: photograph).

IGZO. Taken conjointly, a positive shift of  $V_{fb}$  and  $V_E$  of C-V curve (blue curve in Figure 5b) can be investigated after depositing annealed IGZO/ZnO NPs. This phenomenon can be explained by the schematic diagram of bandgap alignment in Figure S4b in the Supporting Information. The capacitor with as-deposited IGZO has more trap densities at interface. Consequently, the trap states contain negative charges at flat band state, but the trap states capture extra positive charges at inversion state. Comparatively, for the capacitor with annealed IGZO/ZnO NPs, C-V curve (blue curve in Figure 5b) executes positive shift at both  $V_E$  and  $V_{fb}$ . It proves that the major factor of these positive shifts is the increase of electrons derived from ZnO NPs due to the bend of bandgap at IGZO/ZnO NPs' interface.

Lastly, the underlying mechanism of bandgap's bend driven by gate voltage can be explained and quantified through the surface voltage potential of IGZO interface ( $\phi_s$ ). The charge densities at IGZO/SiO<sub>2</sub> interface can be extracted feasibly through classic extraction algorithm<sup>[32]</sup> from above measured C-V curves. By employing Gauss's law, potential along profiles

in the channel can be obtained as:  $\frac{\partial \phi}{\partial x} = \frac{\epsilon_i}{\epsilon_s} (V_{GS} - \phi_s) / d$ , where  $\frac{\partial \phi}{\partial x}$  is the surface potential along the width of the channel,  $\epsilon_i$

is the dielectric constant of insulator,  $\epsilon_s$  is the dielectric of the semiconductor channel and  $d$  is the thickness of the insulator. And  $\phi_s$  also can be calculated according to  $V_{GS}$ . Assuming that charge density in the capacitor is only caused by trap density without taking carrier's mobility into consideration, the densities of different devices' trap states can be extracted in Figure 5c. Due to the natural bandgap of IGZO is around 2.8 eV, when

$\phi_s$  is 2.5 eV (near to  $E_C$  of IGZO), electron's accumulation at interface is saturated (IGZO can be equivalent to a metal electrode for all three devices under higher  $V_G$ ). After performing an annealing process, the defects inside IGZO (such as oxygen vacancy, Zn distortion, and so on) can be improved and diminished. It can decrease the number of trap states whatever  $\phi_s$  near to  $E_C$  or  $E_B$  (valence band) of IGZO. An important finding is that the extracted trap densities of MOS with IGZO/ZnO NPs are also as high as that of nonannealed transistor. It demonstrates that with annealed IGZO and ZnO NPs, many carriers can be transported from ZnO NPs to the transistor's channel through clusters.

In order to research and explain the impact of metal-oxide heterostructure on the QLET's performances, the different sizes of ZnO NPs are utilized as shown in Figure 6a. And the transfer IV characteristics of devices with different sizes of NPs are measured and plotted in Figure 6c. It is evident from that metal-oxide IGZO/ZnO NPs heterostructure plays an important role for modulating vertical transistor. In theory, the smaller ZnO NPs always have stronger spatial quantum confinement, which needs higher energy to create photogenerated carriers. PL intensity of ZnO NPs with different diameter can be checked in Figure S5 in the Supporting Information. The blue shift of QDs' PL peak position can be observed with NPs' diameter's decreasing (20–2.8 nm). The bandgap of ZnO NPs can be broadened from 3 to 4.3 eV with NPs' diameter's gradually decreasing, while bandgap of IGZO is around 2.8 eV. Consequently, without efficient barrier offset between IGZO and ZnO NPs, device exhibit worse electrical performances with a bad SS ( $>5$  V Dec<sup>-1</sup>), threshold voltage ( $>11$  V), and on/off ratio ( $<10^2$ )



as shown in the blue and black curves in Figure 6c. Thanks to this bandgap extension phenomenon with decreasing NPs' size, it can generate electron transport barrier between IGZO/ZnO NPs and achieve better transistor performances.

To further investigate the optical–electrical performance of the QLET, the electroluminescence (EL) intensity (Figure 6d) is measured by varying gate voltage, which demonstrates the effective gate modulation of the light emission. The EL spectra also follows the PL spectra of the QDs, primarily consisting of a 585 nm emission peak and full width at half maximum (FWHM) of 60 nm. This implies that the QLET also possesses unique monochromatic optical–electrical properties of high PLQY QDs with narrower FWHM to achieve high efficiency compared with previous reported OLET listed in Table 1. A negligible finding illustrated in Figure 6d is that the EL spectra of QLET can be broadened slightly under higher gate voltage, because more electrons are driven into ZnO NPs and cause extra excitons' recombination in ZnO NPs. As witnessed in PL intensity of ZnO NPs of Figure S5d in the Supporting Information and EL intensity of QLET with 5 nm ZnO NPs of Figure S5c in the Supporting Information, it can be confirmed that 2.8 nm ZnO NPs have stronger light-emitting due to quantum confinement which are of much wider FWHM. Finally, a conventional structure QLED device is also presented in Figure S5 (Supporting Information) and for comparison (without IGZO on a CNT/glass anode, with the same stack's structure and solution processing). Compared with this device, the heterojunction in the QLET can optimize the charge balance (lower the operating current at  $V_G = 10$  V from 680 to 160 mA cm<sup>-2</sup>) at a high drain voltage. It is because that under higher drain voltage, more electrons are transported into ZnO NPs, which leads to a bend of bandgap of ZnO NPs. It can increase  $E_C$  of ZnO NPs and can prevent from some abundant/noisy electrons from IGZO/Ag source terminal. Consequently, it is possible to regulate the electron's injection via interacted IGZO/ZnO NPs ETLs to QD emitting layers and decrease efficiency roll-off of QLET. EQE is illustrated in Figure 6e, which can be increased by the gate's modulation and reach to another saturated state at high gate voltage. EQE can be maintained at such a high value from 11% to 7% with high 3000 cdm<sup>-2</sup> luminance, which reflects that QLET device exhibits lower efficiency roll-off compared with that of conventional similar QLED and reported OLET device listed in Table 1. These results indicate that the metal–oxide heterostructure helps to maintain superior emissive properties, decrease the power consumption at high luminance, and excellent electrical performance.

### 3. Conclusion

In conclusion, we developed a high-luminance, high-efficiency top-emission vertical QLET device, which can also be easily fabricated and integrated as an efficient module. It can be found from our research that by improving the IGZO/ZnO NPs heterostructure, the vertical transistor structure could generate a basic drain–source current modulation function with high mobility (25 cm<sup>2</sup> V<sup>-1</sup> S<sup>-1</sup>), allowing the luminance of the QLET to be regulated (>10<sup>4</sup> on/off ratio) while the drain–source voltage is fixed. The QLET device we developed, which consists

of solution-processed multilayers, shows excellent illuminating function with large lighting zone (2 mm) while the superior emissive properties (60 nm FWHM) of the QDs is preserved. The peak luminance and EQE measured are up to 8000 cdm<sup>-2</sup> and 11% respectively with a low efficiency roll-off (7% at 3000 cdm<sup>-2</sup>). It is anticipated that the development of QD-based transistors and LED applications based on a vertical transistor structure will be further improved with this promising technology. In particular, a versatile integrated display/lighting device in the future would benefit from the availability of a high-performance top-emission QLET directly fabricated on an opaque silicon substrate.

### 4. Experimental Section

**Bottom Gate Insulator and Zn-Related Semiconductor Device's Synthesis and Fabrication Process:** Bottom gate transistors were fabricated on 2 in. N-type heavily doped silicon wafers (thickness: 400  $\mu$ m, 0.02  $\Omega$  cm<sup>-1</sup>). The standard RCA (Radio Corporation of America) cleaning method was utilized to remove organic contaminants, residual oxide, and ionic contamination. A silicon oxide insulator with a 250 nm thickness was deposited via a PECVD method, and the 60 nm IGZO active layer was formed by an RF magnetron sputtering process. The details of this technique were as follows: a ceramic target consisting of In<sub>2</sub>O<sub>3</sub>:Ga<sub>2</sub>O<sub>3</sub>:ZnO at a ratio of 1:1:2 with a 10 cm target-to-sample distance and Ar:O<sub>2</sub> = 90:4 gas flow ratio (RF power: 160 W, sputtering time: 200 s). Excimer laser annealing with a XeCl 308 nm ultraviolet source was carried out to crystallize and modify the IGZO film, as illustrated in Figure S2 in the Supporting Information. Then, a thin 30 nm silver (Ag) film was sputtered on the IGZO surface as the source electrode and cathode contact for the IGZO and ZnO NP layers. ZnO NPs were synthesized through a sol–gel method utilizing a blend of a 0.1 M zinc acetate dimethyl sulphoxide solution and 0.4 M tetramethylammonium hydroxide ethanol solution. After stirring for 1 h in an ambient atmosphere and centrifuging the products twice, the collected precipitate was dispersed in isopropyl alcohol to create a ZnO NP solution (20 mg mL<sup>-1</sup>). The ZnO NP solution was first spin-coated at 4000 rpm for 40 s and then baked at a certain temperature ( $\approx$ 130  $^{\circ}$ C) for 30 min to remove the solvents. Because the ZnO NP layer was the first spin-coated layer, the roughness and uniformity of this ETL were key for acquiring a high-performance top-emission QLET. Consequently, the morphology of the ZnO NPs is shown in Figure 2b, which displays a uniform 2.8 nm diameter.

**Fabrication Process of QDs-Based Lighting Cell—Spin-Coating Process for QDs and Organic Components:** CdSe/ZnS QDs were purchased from WuHan Jiayuan Ltd., which had a 4.8 nm diameter, 585 nm center wavelength, and 50 nm FWHM, as shown in Figure 2a. QDs with a 10 mg mL<sup>-1</sup> concentration as the emission layer were spin-coated on the ZnO ETL at 1000 rpm for 30 s and baked at 120  $^{\circ}$ C for cross linking. A conjugated polymer (poly[(9,9-dioctylfluorenyl-2,7-diyl)-alt-(4,4'-butylphenyl)]) dissolved in chlorobenzene with an 8 mg mL<sup>-1</sup> concentration was subsequently coated on the QD layer as the electron blocking layer. Finally, a poly(3,4-ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS) electronic ink was spin-coated to act as the hole transport layer at 4000 rpm for 40 s and baked at 145  $^{\circ}$ C.

**Fabrication Process of QDs-Based Lighting Cell—Dry Transfer Process of Top-Emission Transparent CNT Electrode:** An MWCNT dispersed water solution was purchased from a commercial source (Nanjing Xianfeng Ltd.), which used sodium dodecyl sulfate (SDS) as a surfactant to guarantee well-dispersed MWCNTs in water. Then, a polyvinylidene fluoride membrane filter (pore size: 0.1  $\mu$ m) was used to collect the MWCNTs after drying in an oven. Finally, this sample was immersed into pure water for 30 s to remove the SDS surfactant and dried in the oven again. The collected MWCNTs were available for the dry transfer technique, which were first adhered to the patterned PDMS stamp.

Immediately, the PDMS with MWCNTs was impressed on the top of the PEDOT:PSS layer by PDMS stamp with light pressure, where the thickness, transparency, and conductivity of MWCNTs electrode can be affected by the contact pressure and duration.

**Characterization Methods and Instruments:** This QLET's photoelectrical characterization was performed inside nitrogen glovebox with Keithley 4200scs multifunctional semiconductor analyzer and Photo-Research 655 meter with IVL EQE PC terminal measurement system to record electrical and luminance (EQE) data. Single lens camera Nikon D750 with 105 mm macro lens was used to take photos of QLET's lighting images. Moreover, electroluminescence spectrum was detected and plotted by Ocean Optics Maya professional fibre spectra meter. Besides, PerkinElmer LSS photoluminescence spectrometer, Lambda 950 spectrophotometer, Shimadzu SPM9700 AFM, JEOL JEM2000EX TEM and FEI Sirion field-emission SEM were introduced to test PL/transmission spectra and AFM/TEM/SEM photographs for material's characterizations respectively.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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## Conflict of Interest

The authors declare no conflict of interest.

## Keywords

high efficiency, high mobility, large area, light-emitting transistors (LETs), metal-oxide heterostructures, quantum dots (QDs)

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